WHAT IS CLAIMED IS:

1. A decoder for decoding at least one quadrature amplitude modulated (QAM) signal into at least one *n*-bit digital signal, said decoder comprising:

at least one integrator capable of integrating the at least one QAM signal; and

at least one tapped-delay line filter comprising at least one delay element, wherein said at least one tapped-delay line filter is capable of receiving the integrated at least one QAM signal and thereafter outputting a representation of each bit of the at least one *n*-bit digital signal.

2. A decoder according to Claim 1 further comprising at least one comparator capable of receiving the representation of each bit of the at least one *n*-bit digital signal and thereafter outputting each bit of the at least one *n*-bit digital signal based upon a comparison of the representation of each bit to a predetermined threshold.

3. A decoder according to Claim 1, wherein said at least one integrator comprises *n* integrators, and wherein said at least one tapped-delay line filter comprises *n* tapped-delay line filters.

4. A decoder according to Claim 3 further comprising *n* comparators capable of receiving the representation of each bit of the at least one *n*-bit digital signal and thereafter outputting each bit of the at least one *n*-bit digital signal based upon a comparison of the representation of each bit to a predetermined threshold.

5. A decoder according to Claim 1, wherein the at least one QAM signal is capable of being transmitted at a rate of *t*, wherein the at least one QAM signal includes at least one in-phase portion modulated by at least one carrier signal at a carrier frequency of f_c, wherein at least one integrator is capable of integrating the in-phase portion of the at least one QAM signal, and wherein at least one tapped-delay line filter is capable of receiving the integrated in-phase portion of the at least one QAM signal and thereafter outputting a representation of at least one bit of the at least one *n*-bit digital signal.

6. A decoder according to Claim 5, wherein the at least one carrier frequency comprises $n/2$ carrier frequencies, wherein each carrier frequency is equal to a fraction of the transmission rate t/i where $i = 1, 2, 4, 8 \ldots n$.

7. A decoder according to Claim 5, wherein the number of delay elements, m_{in}, of the at least one tapped-delay line filter that is capable of receiving the integrated in-phase portion of the at least one QAM signal equals $(f_c/t)\times 2\times n$.

8. A decoder according to Claim 7, wherein each delay element of the at least one tapped-delay line filter that is capable of receiving the integrated in-phase portion of the at least one QAM signal has a delay of 2Δ, wherein Δ equals $n/(2\times t\times m_{in})$.

9. A decoder according to Claim 5, wherein the at least one QAM signal includes at least one quadrature-phase portion that includes a phase orthogonal to the at least one in-phase portion of the at least one QAM signal, wherein at least one integrator is capable of integrating the quadrature-phase portion of the at least one QAM signal, and wherein at least one tapped-delay line filter is capable of receiving the integrated quadrature-phase portion of the at least one QAM signal and thereafter outputting a representation of at least one bit of the at least one n-bit digital signal.

10. A decoder according to Claim 9, wherein the number of delay elements m_q of the at least one tapped-delay line filter that is capable of receiving the integrated quadrature-phase portion of the at least one QAM signal equals $(f_c/t)\times 2\times n+1$.

11. A decoder according to Claim 10, wherein the at least one delay element of the at least one tapped-delay line filter that is capable of receiving the integrated quadrature-phase portion of the at least one QAM signal includes intermediate delay elements bounded by at least one end delay element, wherein each intermediate delay element has a delay of 2Δ and each end delay element has a delay of Δ, wherein Δ equals $n/(2\times t\times(m_q-1))$.

12. A digital communications system comprising:

a transmitter capable of quadrature amplitude modulation (QAM) encoding each bit of at least one *n*-bit digital signal into at least one QAM signal, wherein said transmitter is capable of transmitting the at least one QAM signal; and

a receiver capable of receiving the at least one QAM signal, wherein said receiver is capable of integrating the at least one QAM signal, wherein said receiver includes at least one tapped-delay line filter capable of receiving the integrated at least one QAM signal and thereafter outputting a representation of each bit of the at least one *n*-bit digital signal.

13. A digital communications system according to Claim 12, wherein said receiver is further capable of outputting each bit of the at least one *n*-bit digital signal based upon a comparison of the representation of each bit to a predetermined threshold.

14. A digital communications system according to Claim 12, wherein said receiver comprises *n* integrators capable of integrating the at least one QAM signal, and wherein said receiver includes *n* tapped-delay line filters.

15. A digital communications system according to Claim 14, wherein said receiver further comprises *n* comparators capable of receiving the representation of each bit of the at least one *n*-bit digital signal and thereafter outputting each bit of the at least one *n*-bit digital signal based upon a comparison of the representation of each bit to a predetermined threshold.

16. A digital communications system according to Claim 12, wherein said transmitter is capable of transmitting the at least one QAM signal at a rate of *t*, wherein the at least one QAM signal includes at least one in-phase portion modulated by at least one carrier signal at a carrier frequency of f_c, wherein said receiver is capable of integrating the in-phase portion of the at least one QAM signal, and wherein at least one tapped-delay line filter is capable of receiving the integrated in-phase portion of the at least one QAM signal and thereafter outputting a representation of at least one bit of the at least one *n*-bit digital signal.

17. A digital communications system according to Claim 16, wherein the at least one carrier frequency comprises $n/2$ carrier frequencies, wherein each carrier frequency is equal to a fraction of the transmission rate t/i where $i = 1, 2, 4, 8 \ldots n$.

18. A digital communications system according to Claim 16, wherein the number of delay elements, m_{in}, of the at least one tapped-delay line filter that is capable of receiving the integrated in-phase portion of the at least one QAM signal equals $(f_c/t)\times 2\times n$.

19. A digital communications system according to Claim 18, wherein each delay element of the at least one tapped-delay line filter that is capable of receiving the integrated in-phase portion of the at least one QAM signal has a delay of 2Δ, wherein Δ equals $n/(2\times t\times m_{in})$.

20. A digital communications system according to Claim 16, wherein the at least one QAM signal includes at least one quadrature-phase portion that includes a phase orthogonal to the at least one in-phase portion of the at least one QAM signal, wherein at least one integrator is capable of integrating the quadrature-phase portion of the at least one QAM signal, and wherein at least one tapped-delay line filter is capable of receiving the integrated quadrature-phase portion of the at least one QAM signal and thereafter outputting a representation of at least one bit of the at least one n-bit digital signal.

21. A digital communications system according to Claim 20, wherein the number of delay elements m_q of the at least one tapped-delay line filter that is capable of receiving the integrated quadrature-phase portion of the at least one QAM signal equals $(f_c/t)\times 2\times n+1$.

22. A digital communications system according to Claim 21, wherein the at least one delay element of the at least one tapped-delay line filter that is capable of receiving the integrated quadrature-phase portion of the at least one QAM signal includes intermediate delay elements bounded by at least one end delay element,

wherein each intermediate delay element has a delay of 2Δ and each end delay element has a delay of Δ, wherein Δ equals $n/(2 \times t \times (m_q - 1))$.

23. A method of decoding at least one quadrature amplitude modulated (QAM) signal into at least one *n*-bit digital signal, said method comprising:

integrating the at least one QAM signal; and

filtering the integrated at least one QAM signal, wherein filtering comprises passing the integrated at least one QAM signal through at least one delay element aligned in series, wherein an output of each delay element is summed together with the integrated at least one QAM signal to thereby output a representation of the at least one *n*-bit digital signal.

24. A method according to Claim 23 further comprising receiving the representation of each bit of the at least one *n*-bit digital signal and thereafter outputting each bit of the at least one *n*-bit digital signal based upon a comparison of the representation of each bit to a predetermined threshold.

25. A method according to Claim 23, wherein the at least one QAM signal is capable of being transmitted at a rate of *t*, wherein the at least one QAM signal includes at least one in-phase portion modulated by at least one carrier signal at a carrier frequency of f_c, wherein integrating the at least one QAM signal comprises integrating the in-phase portion of the at least one QAM signal, wherein filtering the integrated at least one QAM signal comprises passing the integrated in-phase portion of the at least one QAM signal through at least one delay element aligned in series, and wherein an output of each delay element is summed together with the integrated in-phase portion of the at least one QAM signal to thereby output a representation of at least one bit of the at least one *n*-bit digital signal.

26. A method according to Claim 25 further comprising determining the number of delay elements of the at least one tapped-delay line filter that is capable of receiving the integrated in-phase portion of the at least one QAM signal before filtering the integrated at least one QAM signal, wherein the number of delay

elements, m_{in}, of the at least one tapped-delay line filter that is capable of receiving the integrated in-phase portion of the at least one QAM signal equals $(f_c/t)\times 2\times n$.

27. A method according to Claim 26 further comprising determining the delay of each delay element of the at least one tapped-delay line filter that is capable of receiving the integrated in-phase portion of the at least one QAM signal after determining the number of delay elements, wherein each delay element of the at least one tapped-delay line filter that is capable of receiving the integrated in-phase portion of the at least one QAM signal has a delay of 2Δ, and wherein Δ equals $n/(2\times t\times m_{in})$.

28. A method according to Claim 25, wherein the at least one QAM signal includes at least one quadrature-phase portion that includes a phase orthogonal to the at least one in-phase portion of the at least one QAM signal, wherein integrating the at least one QAM signal comprises further comprises integrating the quadrature-phase portion of the at least one QAM signal, and wherein filtering the integrated at least one QAM signal comprises passing the integrated quadrature-phase portion of the at least one QAM signal through at least one delay element aligned in series, and wherein an output of each delay element is summed together with the integrated quadrature-phase portion of the at least one QAM signal to thereby output a representation of at least one bit of the at least one *n*-bit digital signal.

29. A method according to Claim 28 further comprising determining the number of delay elements of the at least one tapped-delay line filter that is capable of receiving the integrated quadrature-phase portion of the at least one QAM signal before filtering the integrated at least one QAM signal, wherein the number of delay elements m_q of the at least one tapped-delay line filter that is capable of receiving the integrated quadrature-phase portion of the at least one QAM signal equals $(f_c/t)\times 2\times n+1$.

30. A method according to Claim 29, wherein the at least one delay element of the at least one tapped-delay line filter that is capable of receiving the integrated quadrature-phase portion of the at least one QAM signal includes

intermediate delay elements bounded by at least one end delay element, said method further comprising determining the delay of each intermediate delay element and each end delay element after determining the number of delay elements, wherein each intermediate delay element has a delay of 2Δ and each end delay element has a delay of Δ, and wherein Δ equals $n/\left(2\times t\times *(m_q-1)\right)$.